H.264 HD DECODER

Exceptional. Scalable. Robust.

1080P60. 4:2:2. 10BITS.

OVERVIEW

The H.264 Decoder Core is a highly optimized, high resolution decompression engine targeted primarily at FPGAs. It is well suited for various applications ranging from broadcast and professional video to high end consumer electronics.

The decoder design is fully autonomous and does not require any external processor to aid the decode operation. The IO interface comprises of an input FIFO and an output frame buffer. Decoded data can also be provided on a serial bus with embedded sync information. The decoder requires DDR SDRAM to store reference pictures.

The decoder solution is available either as a FPGA netlist or in source code format and can be customized to meet the requirements of end users.

KEY FEATURES

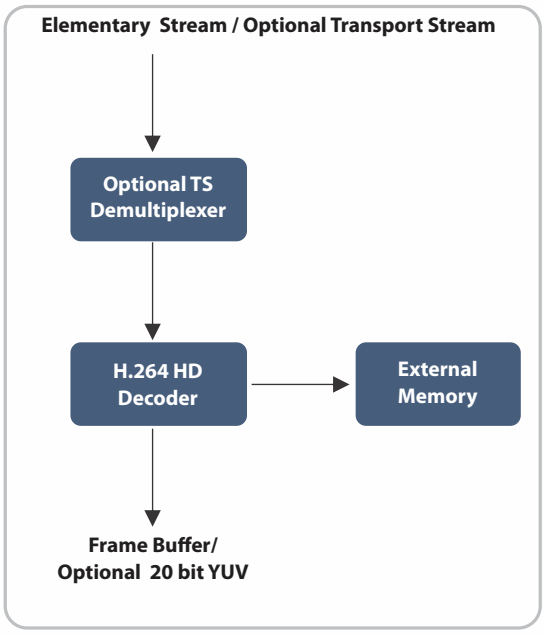
- Fully standards compliant - tested with ITU-T & other industry standard test suites
- Robust error handling, resilience & concealment
- Processes metadata related to closed captions, AFD & picture timing
- Seamless switching between streams encoded with different settings including different resolutions, chroma formats and bit depths
- Extensive options to customize the source code via use of parameters
- Single chip solution with no processor requirement
- Supports progressive and interlaced formats
- Supports both CABAC and CAVLC Entropy coding
- Easy to integrate and hence faster time-to-market

FPGA RESOURCES

FPGA	LUTs	BRAMs	DSPs
Kintex Ultrascale	33,000	91	112

- 1920 x 1080p60, 422, 10-bit, 40 mbps CABAC, 80 mbps CAVLC decoder
- Does not include memory controller, display controller and TS demultiplexer

BLOCK DIAGRAM



SPECIFICATIONS

Standard:	H.264/MPEG-4 Part 10 (ISO/IEC 14496-10 & ITU-T H.264)
Profiles:	Constrained Baseline, Main & High profiles
Video Resolutions:	Up to 1920 x 1080
Frame Rate:	Up to 60 fps
Bit rate:	CABAC Bitrate: 40 Mbps. Scalable to 80 Mbps CAVLC Bitrate: 80 Mbps. Scalable to 160 Mbps
Chroma Format:	Monochrome, 4:2:0 & 4:2:2
Precision:	Bit depths from 8 to 10
Input Format:	Elementary or Transport stream
Output Format:	Decoded pictures in frame buffer. Optional serial output with embedded sync information
Latency:	Ultra low latency of 10 ms
Codec Flavors:	AVC – Ultra, H.264 4K, XAVC
FPGA:	Xilinx Ultrascale, 7-Series and 6-Series FPGAs Altera devices are also supported. Contact us for the information.

DELIVERABLES

- Source Code or Netlist
- Simulation Model
- Hardware Test Platform
- Build Scripts
- Test Reports
- User Manual
- Design Documentation
- Constraint Files
- Test Benches
- Support for one year

APPLICATIONS

BROADCAST

VIDEO WALL AND DIGITAL SIGNAGE

HIGH END CONSUMER ELECTRONICS

AEROSPACE AND DEFENSE

TEST & MEASUREMENT EQUIPMENTS

MEDICAL

VYUSYNC

VYUsync develops high performance video processing intellectual property cores. Our products cover a broad range of standards and are optimized for deployment across a wide array of segments including Contribution, Production, Distribution, Medical and Defense. VYUsync also develops hardware modules which incorporate the IP cores in order to allow our customers to reach market faster.

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