HEVC HD DECODER

Cutting Edge. Flexible. Resilient.

1080P60. 4:2:2. 12BITS.

OVERVIEW

The HEVC HD Decoder Core is a highly optimized video decompression engine targeted primarily at FPGAs. It is well suited for various applications ranging from broadcast and professional video to high end consumer electronics.

The decoder design is fully autonomous and does not require any external processor to aid the decode operation. The IO interface comprises of an input FIFO and an output frame buffer. Decoded data can also be provided on a serial bus with embedded sync information. The decoder requires DDR SDRAM to store reference pictures.

The decoder solution is available either as a FPGA netlist or in source code format and can be customized to meet the requirements of end users.

KEY FEATURES

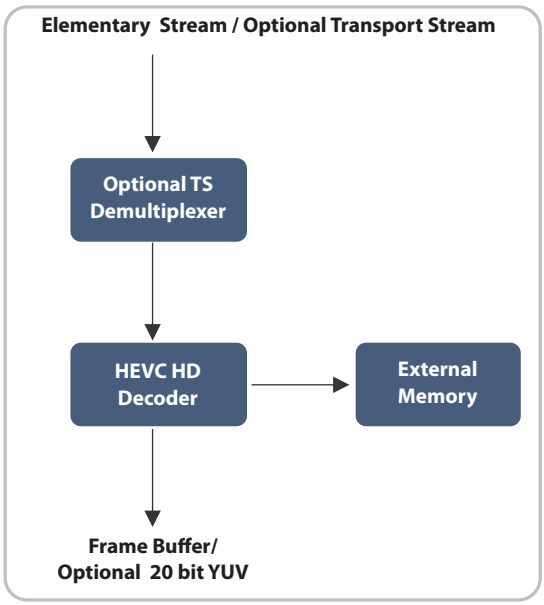
- Fully standards compliant - tested with ITU-T & other industry standard test suites.
- Robust error handling & resilience
- Processes metadata related to closed captions, AFD, timing & HDR
- Seamless switching between streams encoded with different settings including different resolutions, chroma formats and bit depths.
- Extensive options to customize the source code via use of parameters
- Single chip solution with no processor requirement
- Optimized resource utilization
- Easy to integrate and hence faster time-to-market

FPGA RESOURCES

FPGA	LUTs	BRAMs	DSPs
Kintex Ultrascale	55000	209	185

- 1920 x 1080p60, 422, 10-bit, 75 mbps decoder
- Does not include memory controller, display controller and TS demultiplexer

BLOCK DIAGRAM



SPECIFICATIONS

Standard:	HEVC/H.265 (ISO/ IEC 23008-2 and ITU-T H.265)
Profiles:	Main, Main10, Main 12, Main 10 4:2:2 and Main 12 4:2:2
Video Resolutions:	Up to 1920 x 1080
Frame Rate:	60 fps
Bit rate:	75 Mbps. Scalable to 150 Mbps
Chroma Format:	Monochrome, 4:2:0 & 4:2:2
Precision:	Bit depths from 8 to 12
Input Format:	Elementary or Transport stream
Output Format:	Decoded pictures in frame buffer. Optional serial output with embedded sync information
Latency:	As low as a few microseconds
FPGA:	Xilinx Ultrascale and 7-Series FPGAs Arria-10 support coming soon

DELIVERABLES

- Source Code or Netlist
- Simulation Model
- Hardware Test Platform
- Build Scripts
- Test Reports
- User Manual
- Design Documentation
- Constraint Files
- Test Benches
- Support for one year

APPLICATIONS

BROADCAST

PROFESSIONAL VIDEO

HIGH END CONSUMER ELECTRONICS

AEROSPACE AND DEFENSE

AUTOMOTIVE

MEDICAL

VYUSYNC

VYUsync develops high performance video processing intellectual property cores. Our products cover a broad range of standards and are optimized for deployment across a wide array of segments including Contribution, Production, Distribution, Medical and Defense. VYUsync also develops hardware modules which incorporate the IP cores in order to allow our customers to reach market faster.

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